UNIT-I

Electrical measurment and Instrumentation coveres:

I Electrical parets:

ij fleotroniu peuto

- · Babic of measument system
- · Error Analysis
- · Analog Instruments . EMMC
  - · ESY Electrostation
  - · Mermel Instruments
  - · Rectifier type Inst
- ·Measurment of Results
  - D.C. Boidge
  - Measynment of L, C, M. mut. And
  - A.C. Bridge
  - · Measurment of power
    - D.C. power measurment
      - A.C. power measurment
    - · Measurment of energy
      - · Potentometer
      - Instrum. TIf
      - · power factor metch
      - · flux meter

Electronic pent

- · Q-meter
- · CRO
- · DVM
- · Transducez

In each and every field of engineering, sciences-there is repuirement of various quantities such as physical, mechani cal, electrical, chemical, thermal etc All 84th measurments are required for mantaning and observational analysis for valuable necords, research and development.

? what is the purpose of measurment:

The purpose of meanument is to present measured value

to numerical values. e.g. - when we have to measure any phypical quantity, its output should be in numerical value (if it is

To sumerice value then it is very early to understand for everyone)

to measure weight - first some numeric valle When we have 10 -> numeric value kg its unit. then its unit e.g. lokg. 18 there and

of Dist -E E Etc Curront

98 ° etc. etc Temp

-> hohet is measured value, what is true velue, Diff.

! Measured value: -> Any value or any reading calculated from measurment system or measuring roust-sument 18 known as measured values.

2. TRUE/values: > Arry value calculated from nated values?

ACTUAL

18 known as torus values.

Example! Let us we are hering a motor (may be d-c/a-c) with its neted speed 3000 spins. Then Its NT = 2000 spins but we can measure the speed with the neep of Pachometer. If tachome ter reading is 2998 menting -2998 copin 1 Measured from the reading is 2998 -2998 = 02 (Error) 2 Measured Gramply

Error: + It is the deviation of measured value from the @. Trule - , Tachometer - , Measured value true value 5ystem -> Measuring Instrument -> System oretput measured value Error = S = Am - AT JO or Error = System ofp - System /p of AM>AT => Error = +ve AM LAT => Brosor = -VR Example: If we are having two metrument: Inst. A 2 Inst B men which of the following methuments is make quality metrument? Frat B Sp= 10 Amp SiA = 1 amp (as only A B Dnly B & Both A2B & None of above [Till we are not award about the true value of each instrum.] bez of posufficient data] 135 | we can't comment 135 | till we don't know about that max masky [9] three study got marks A 3 also \$ The quality of any onstouments is decided by of relative static from or Y. Fresting beene (FE) 1. RSE of 1- Relative Static Errors  $=\frac{Am^{-}A_{T}}{AT}\times 100 = \frac{S_{A}}{A_{T}}\times 100$ Limiting Ensor = (AM-1) XION - @

Now I will mention the value of true value AT of each metalinent:

most A

$$S_A = 1 amp$$
 $A_T = 2 Amp$ 

Frot B

$$\frac{1}{\sqrt{-RSE}} = \frac{SA}{AT} \times IDD$$

$$= \frac{1}{2} \times IDD$$

Merefor the quality of 8 most is

Also, if also asked about to calculate accuracy.

Here = 
$$100-1$$
 =  $99/$ .

=> Inst B is more Quality
Frot.

Conclusion! - The quality of the motherment is always decided by / relative static error, the error is always expressed in term of true value of the valuable.

The Art. I

BASIC Concept on Measurement: In each and every field of 8 cience engineering, there is generally reprinement of various quantities such as physical mechanical electrical, chemical, therenal etc. All such measurments are repuired too maint aring the and observational analysis for valuable secords. research and developments. There are various methods of for measurments that we study in measurment & Instrumentet! The massiscount is basically a composizion of given guentity with a sterndard fixed quantity what is a prederined standard). The fixed quantity me taken as the basic is called a linit. The MEASURMENT can be defined as the process of compession of given quantity in terms of its standard quantity or its basic unit. " The process by which one can convert physical Methods of measurments: >> if Direct method in Indirect metho parameter into meaningful number." I. Direct Method: -> The unknown quantity 18 directly compared with the known quantity. for e.g. (Simply hight & weight) 2. Indirect measurment: -> In this method, either the current or voltage is converted into mechanical deflecting torque by means of electromechanical emergy conversion. e.g. Ammeter Noltmeter.

+ for example we use anneter for massurment of current and vollmeter for voltage. (There is a deflection in pointer try from to some value—this detection is due to supply of currentled-c value) to the connecter & volumenter). · Direct method is not suitable for electrical circuitory.

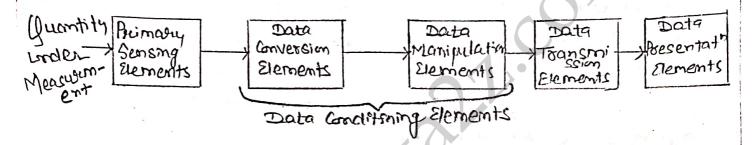
Elements of Gonerelized Measurement System: -> It is important to have a systematic organisation and analysis of measurement system. Manly the measurement system contain three man functional elements:

1. Primary Sensor Elements

2. Vouciable americian Elements and

3. Data presentation elements.

The function of each exponts are as under:



I Poimary Sensing Elements: -)

The quantity under measurement makes its first contect with the primary sometime elements. The quantity to be measured is first detected by promary sensing element the quantity detected by the primary sensing element may be pressure temperature, any mechanical quantity (that is non electrical quantity (signal) is converted into electrical quantity if with the help of transducer. Transducer converts the physical quantity detected by primary someoned element into electrical signal.

2. Data Conversion Element! > Now, the output obtained from preinting General! > Now, the output obtained from preinting General 18 is electrical form such as a completed Eyeken of measurement such output vigned will have to be converted from analog to digital which 18 dane by variable Conversion element.

Thus RID converted 18 data conversion element.

3. Date Manipulation Elements. The function of this element the manipulate the opposed. Manipulation of the Dignal means changing its in numeric value for example an amplefer. An armplifter amplifter the magnitude of the incoming original while relaining its original nature. A variable manipulation element am be connected befor or after Data Conversion element. If connected after Data residual element, it is used to amplify the incoming, whereas if connected before then its functions as an attenuator.

The trongetucer used earlier converts the data in a small expert, so that the manipulation element com amplifies the signal for its further from them. (of data). I late on its from it convert other former on the matrix possible by amplifier and attentivator. Ebc3 the tronsduced have generated a small expect that con't be displayed directly).

4. Data Transmission Elements! I sometime it is noticed that where we performing the experimental work or date manipulation them we have to process the the duta to any other place. So if clocation of standard are not metching so that we have to transmit the date. The data transmission transmits the data from one stage to another if the elements of the system are physically separate.

5. Data presentation elements: > The transmitted data is used for the purpose of monitoring and controlling purposes. The data presentation elements presents the information in proper form to the end user for the effective analysis. If data is to be monitored then visual ouspray displays clevices are used as presentation element. Readers, cameras or magnetic tapes are used for recording of data.

for controlling and analysis a data pregentation element consist of Computers, microcontrollers or microprocessors.

(E)

Instruments and measurement system! I he instruments are used for the measurement with means of all terming quantities or waveables. The instruments are consist of angle unit which gives an output reading or signal according to the unknown variable (measurement) applied to it. A measuring instrument may consist of saveral separate elements. There elements may consist of saveral separate elements. There elements may consist of transducing element which convert the measurement of an analogous form. The analogous signal is then processed by some informations means and then fed to the end device to present the results of the measurement for the purpose of display and control.

Types of Electrical measuring Instruments! ->

- 1 Active & Passere Jost 2. Null of Deflection type Joset.
- 3. Analog & Agritce Inst. 9. Absolute & 2ndary Instruments.

Secondary Inst

a. Indicating Inst.

5. Integrating

c. Recording

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Report to ments mouse 15

Noise: - in an Electronic System:

· In electrical terms, noise may be defined as immembed form of energy which tends to interfere with the proper reception and reproduction of transmitted Signal. Indicate I outside I to Marie I outside I to Marie I outside I to Marie I outside I outside I outside I original I noise is immembed signal which interfere with original message signal and corrupts the parameters of the message

signal.

It is likely to be entered at the channel or recieven etc.

Amplifued Noisesignal

no pattern and no constant fregamplit.

-> It is quite random and impredictable. impact of signed has it

-> Measures are usually taken to reduce it, though it con't be completely eliminated.

To improve the system performance, usually we want to eliminate the noise, but it is difficult to remove out, it can be reduced, as much as possible.

There are some examples of noise such as

Noise can observed in radio receiver, in receiver saveral signal electrical disturbances produces noise and therefore modifying the repaired signal in an unwanted form. so in case of radio receiver the noise may produce HISS type of pattern (at the output of loudspeaker)

-> If we talk about Ty receiver, the noise may produce show the snow actually suproimposed with the picture 0/p. So of TV receiver SNOW and FLICKER are the kind of moise in core of TV receiver

7 BUZZ Sound almost telephonic conversation.

ANOISE is a factor which is going to impact a lot on eignal quality and hoise may limit the performance of the electronic or the communication system

Effects of Noise:

· Noise Limit the operating range of the system

July of the state of

PORTE A LONG CONTINUE OF LONG TO A SHOP

radio received the control of

AND THE WORLD STORY

so so my the comment of the last of

· Moise affect the sensibility of the necessers.

Noise in An Electronic System: >

In electrical terms, noise may be defined as an unusquited form of energy which tends to reventer with the prosper reception and reproduction of transmitted rignal. for example in necesivers, renoval electrical disturbances produce noise and thus modifying the required Signal in an unwanted form. In T.V. necessare noise may produce 'snow' which becames superigniposed on the picture orutput. In actual the noise may brait the performance of the a Communication Eyeken.

# Noise 18 an unwented, handom and undeterministic electrical signal, which interfere with reception and reproduction of transmitted signal. why Noise can affect sensitivity of secences. and con also cause reduction in B.W.

Classification of Noise: -> There are marry two ways of crassifying the noise as under: I External Moise 2. Internal Noise.

The noise created oretside the neceiver 1. External Moise! 18 called External noise. The external noise com't be analysed quantitatively that's why it connot be controlled. They to reduce the effect of external noise, the only way is to shift the communication system to other place or

Location which has comparatively smaller noise. Thus due to this reason, the sattelite earth stations are generally Located in noise free valleys.

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External Moise com be classified as:

Almospheric Moise 2. Extrateszaistrial Moise

iii) Industrial Moise.

If thospheric Moise: + Almospheric Moise which is also called static, is produced by lightning discharges in thunderstorm and other natural electrical distrubences which occurs in atomorpher Atmospheric noise contains spurious radio agrads which are straightful over a wide range of frequency.

This is trandom and spread over Af spectrum used for broadcasting. It has been absenced that the steld when the steld interest at atmospheric noise values approximately inversely with frequency. This conclude that large atmospheric with frequency bands noise is produced in tow and medium frequency bands noise is produced in tow and medium frequency bands noise is produced in the VHF and UHF bands. Thus whereas very small noise in the VHF and UHF bands. Thus house becomes loss at frequencies above so MHz because noise becomes loss at frequencies above so MHz because house frequences are united to too.

Extraterristrice Moise: > the extratorristrial notre 18 furthere
subdivided as a) Solar Holse y Carmic Moise

a) Solve Noise: Jolan Noise is produced by the radiations emitting from Sun because sun is a large body at a very high temp (over 6000°C).

b) Cosmic Noise: The cosmic Noise is produced from distort!

b) Cosmic Noise: The cosmic Noise is produced from distort!

tours (es they have high temperature). Also called black hody noise or thermal noise and is uniformly distributed over the entire sky.

C.9 noise in substation (power tit). also area in indust noise.

INTERNAL MOISE: -> Internal noise 18 that type of moise which 18 Demerated roternally the circuit or within the system or roceiver. Moise created by the active/persone devices found is heceivers. Internal noise may be treated quantitatively and can also be reduced or reminized by proper system design. This nois is proportional to B.W. over which it is meanined. Internal noises are further caregorised into force ing types!

Thermal Noise: -The thermal noise or the white noise inhich 18 generator in a nexistor or the resortive companent of the circuit. It is due to the rapid and random motion of molecules (atom) elections) moide the registence.

Noise generated by a resister 18 proportional to its absolute temperature and bondwidth over which per noise is measured. I

> Pn X TB = KTB K 18 Boltzman's Cout = 1.38x 10-27 T/K T = Absolute temp, K= 273+2

B = Bondwidth, Pn = Noise power output of Yn = JUKTBR Ris resignee

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Shot Moise: - mis type of noise is caused by short effect in all amplifying devices and active devices. This type of holse 18 caused by London variation in the aboutal of election or holes at the output electricles of ampli-Tying acrices.

e.g. For a diade, shot noise current is given by

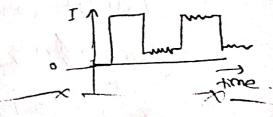
where in = 7.m.s. shot noise current. e = Electron charge = 1.6×10-19c

ip = Direct diade current, B = Bendwicth of system.

3. Flicker Noise: - OR LOW frep. Noise: -> 1/4 Noise

- Mis type of noise is observed below few Khz forg.
- Its spectral donsity decreases increases with decreases in frep. Mus known as If noise.
- Mrs moise becomes significant at feet tower than 100 Hz

Burst Noise: -It consist of sudden step like transition bia two or more describe voltage or current levels, order of saveral hundered microvott. Current Lest from saveral ms to s.



5'ignal Conditioning Christs: -> In goneralized measurment system, discussed about the various data conditioning elements such as poinary sensing of sensing elements, Data conversion elements, Data momipulation elements, Data transmission elements etc etc & All these are data conditioning elements. Let us consider we are having Diff. Interespediate blocks:-Analog in put -> Tromeduces ) Signal coorditioning stage output of stage in put stage Intermediate Stage Gigoral Conditioning 18 the intermediate stage 6/w output and injuit Gage. · what does the intermediate etage = it modifies the output of tronsdu cer according the outpout repuirement. => It modifies the transducer output according to the output stage. · various types of input may be · physical, themsel etc. Here transducer - one physical quantity to another phy. Quant-Here we will discur about electrical/signal as it easy to modify it, we diank modify it, attenuate, amplify etc. so here if physical quantity is converted into electrical signed then it is to be done by at transducer. Suppose at the op of transducer we are getting Analog esp. and at the output stage use are having digited of p (that to be measured). Now is it possible to measure the onalog of p (of transducer) by a digital (output stage) = No

Now this analog output (of transducer) is to be converted to digital by a signal conditioning circuit. Merefore the function of signal conditioning -It modifies the transducer output according to the output stage". Varcious (function" of stones conditioning: )
Mainly there are two processes so signal conditioning directs: "I timean process I'l Non Imean process Linear process Non Inear process Amplification Modulation Differentiation Demodu lation Integration Clipping Addition Clamping etc. Subtraction etc. It persons both (linear and Non Inear) funct) for example it we have to anyplify a signal If we are amplifying a signal with small value 0.000/A. -> The mysem is stanty with 2000 men this signal will be amplify. Now multiplied by Scale tactor & Divide Later on /After measured.

Op-Amp also perform the same functions (Also performs the operations also)

It is also a figural conditioning chet in Add etc. Yorious Conversion: I from organal and tommy - Ex-thamocomple is Active Homodue, , no need of external source S.C. or amplifies the amplitude

Fitering: ) Suppose we are having a naisy signal, of we will Fillerthis signal gy we filtering pass ;+ in signed andituring Notse Leduced. Excitation: - Otrain gauge, RTD ] Passive tronsducer. -) which needs external power source for => S.C => Armp, Diff, hoster, Add, sult etc. (power) source to the konsdul power source for Types of signal conditioning - (1) D.C. Signal condit 2) A-C (1) D.C. Signal Conditioning Power D.C. Excts 1,2,4 Source measuhands Supply 1 Transducer Calibration Bridge D.C. and seroing >0/p pass Amplifica network #Her input age signal and stage · This is block diagr. for D.C. signal anditioning. Stage first of all ip to the trand - ip may be V, I, for any other phy Quat which is to be measure -> that we will five in measuremd · Now this transducer will convert it into Electrical signal ( Tooned are also two types - phys Q to El -> Elect Tounsolven and Electrical to non physical => I Invoise Toury. . Vorious block/parts in the signal conditioning stage will convert the of p of the transducer as per the reprinted autput at output stage. we have to madify the signed accito off stage.

The output of the transducer will be given to the produce, Strain Grange - Two cases - Balanced & Unbalanced · Example using wheat some Bridge Inbalance Godfin unbalanced 1) Balanced -apply Steam Gauge If we will apply strain 010 Volt >0 dimension will change 2 it will imbalance Vo =? on one along RIR4= BR3 | Vo=0 · we have to balance the wheatstone bodge by applying potentiameter on one our

the exp of the is over to bodge.

There stown Grange is used as a Here stown Grange is used as a Here stown Grange is balanced is balanced through potention eter.

if it is balanced, then Vo=0

Thow if we are applying stowng gauge on any one arm or if we apply free, the the dimensions will be automatically changed.

I will be unbalance, Remaining (7) will be some. Now it will

Rim Tike Baloneal
Vo =0
Right Right

unbelonce

who strain

Crange

Vo=?

be tonbalanced cond:

The output will be unbelonized -> this will be measured by calibrating & soroing now

## Calibrating 2 serving 11/w:- To measure unbalanced output of bridge clet.

- · Now unbelonced output of bridge cut is measured
- · Now this unbalanced oup will be given to d.c. ampl
- It will amplify the opp that is to be measured easily
- · Now it will be supported to Low pan filter.

Low Pass filter -> it will bemove the high frequency components (also heduce the noise signal)

Adv of D.C. Strong amplificies tea o m DC

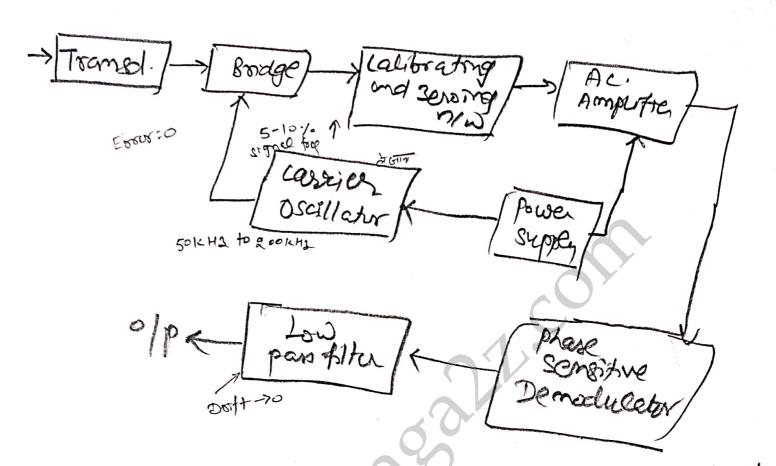
1) It is easy to calibrate at Low free.

D9+ 18 able to recover from an overload conds.

Disadv: - Doift / Error in reproduction lity with same .

Low frequency suprisus eignal individual polony individual polony Drift - Due to D.C. group 4 for use - there is a dust in experior. - that is unconted to grad -)

How to Remove this Doiff of by using A-C.
-Bonco conclitioning



- · Tons 18 block diag. for a.c. signal and timing time is then through casson
- · Electrical signal is provided through the Transduction oscill
- · Tore of +/d" is given to Bridge. -> In prev. case there was a d.c. same on Boidge but here we are gring corrier excillator (through the power supply - it les the frequency) it will add the frep. (in prev. reduced fry. (300 10 D.C).
  - Now it is easy to compare the opp from the ampletion. before worky carrier oscillator it was not after to comp
    - . It will les the 2 =) orginal will be from thed in betta in Dic signal unditining - ) toy Low - weak signed and phase sonsitive Demodulator: - fry was added by course oscillator phase sonsitive Demodulator: - Now it will remove / belonge the frep.

Chez we didnot need the added frep. original To mantain the signal Oreality
Now there will be original signal and this signal will be passed through LPF
- Noise will be reduced - we will obtain a pune signal.

late Acquisition System: - Acquisition -> Acquiring/ collecting some-

- -> Collecting the data from real / physical world and converting that data note signals that can be processed by computers for the use of engineers/scientist.
- -> Data acquisition system is an information agreen that collects, stores and distributes information.
- -> It is used in industrial and commercial electronics and environmental and scientific epuipments to capture electrical signals or environmental conditions on a compater device.
  - -> shis system capture, stone I procen the data, therefore it includes different tooks and technologies that are deligned to accumulate the data

Dotte Acquition System Consist of: (DAS OR DAQ)

→ Senson

-> Date Honelling.

-> Signal Conditioning

-> Associated tronsmission, storage

-> Data Conversion

and Display devices.

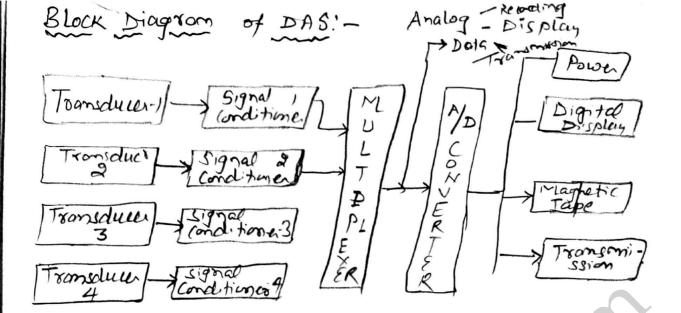
The data aequition eystem involves-acquiting the data processing over it storney the data and then transmitting that data

-> Data processing
-> Multiplexing

50, for the captury of data it is having the senson, for processing over their data is signal conditioning, data conversion, deta processing, multiplexing, data handling conits =>After there for the storage, for the display for the transmission of data we are having different devices.

Broadly we can say that, it consist of these blocks or reparate units and function of these unit is Ist acquiring the dath, doing the process over it and then tooks visous and display. Block dragion of such on DAS or function for each units / Blocky are: -

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mis 18 the black diagram of data acquisition system, that browned of main units and subunits combined to form a tolgger unit. The function of each black are as follows:
TRANSDUCER: -> | Senson from physical world or environment.

TRANSDUER: -> / Senson from physical world or environment.

gt is used to convert the physical Quantity

moto electroical quantity. Also can bey used

to measure directly the electroical quantity

voltag ament fig. Resist.

I signal Conditioner. Earlier the transduce acquire the deta/signal from physical world metal this and convert it into electrical transfer and convert it into electrical transfer and where electrical transfer amplitude hos to inchess duce are weak trignal (with Low amplitude hos to inchess e their amplitude, amplification has to be done, also if the rignal is containing unwanted transfer or noise is there so to be remove there noise and unwanted there so to be remove there noise and unwanted trignal either alteration, filteration of those soignal is being done. Merefore we can say that all therefore function are done in signal analytication unit.

\* To make the signals strong, various signal conditions ones are used

-> Amplifier

-> filter

- Modifier. etc.

## 3. Multiplexer: -

It accepts multiple analog inputs and provide a single output signer according to the repuirement of signer. At the imput of the multiplexer various imputs are then and a single output is there at the output end.

4. A/D Converter: -> It converts the analog data to the digital onetput.

Why we convert into digital => · Easy proceeding

· Easy trongmission, edigital data is

· Digital Display 2 storage

of digital data is easy.

A for many electronic system, only the digital data is being used, but the transmission of digital data is very fast, also its processing is very fast, so in most of the areas digital form of data is used so conversion becomes very impostant thank hence AID converts the analog data to the digital data

- Easy to process

, " transmit

processing over digital

Job due to easy display & storage 7 > Digital data capine Less space, we are getting digital reading so the error are reduced. Therefore we can say that the digital data system has

more advantageous than analogidata. So there is a need of analog to digital data conversion that is done by A/D converte.

5.	Recorders & Dispolar Devices: ->
	After conversion the data, the teansmission, display and stonege
	After conversion the data, the teansmission, display and stonege of data 18 reprined/needed for that purpose we are having
	the Recorders & Display devices.
٠	Data is displayed in suitable form in order to monitor

the imput signals. So example of display devices an

→ Oscilloscope

-> Numerical Displays -> Panel meters

Becording con also be done (for future use

-) Data can be either permonently or temperanely stoned on necorded. e.g.

· Optical recorders

· Disc

Litraviolet recorders

· Tapes

. Stylus and mk recorders

\* The data acquirion system based on the output (provided) by it is divided into two types: - if Analog data Acq System ij Digital

\* Objectives of Data Acp. System:

1. Must acquire the necessary data at correct speed.

2. Use of all data efficiency to inform the operator about the state of the orput

(b) ectores! must be able to summerize I store dots for alagmoss of operation and necod purpose -> must be Flexiky and cupable of being exposded for fature repursement. -> might be seliable and not have a down time greater francos) oily -s must provide on expective human Communication by stem ( must be easy to need / under stand) not my readeble I bound on output D/A. I Diostel are more implex than Analog. both is ten of toples. Notomont Analy MS \* Molistoical areas plant from thep Scientific ereas Beroppele bromedical Freld

Telemetry

Hnalog System Vesign Definition Analog design in the context of integrated circuit design is a discipline that focuses on the execution of circuits that operates in and are optimized for Continuous time-domain behaviour. Typhical objectives of analog dosign include :-· Signal fidelity · Amplification · Filtering > When term "integrated circuit design" is mentioned, most people think of the design of complex microprocesses. These circuits are designed using digital design techniques, Which focus on the propagation of discrete values, i.e. "ones and zeroes". => Importance of Analog Vesign Since all the basic devices in an IC respond to continuous time stimulus, analog design forms the foundation for all IC design. Modern IC technology presents many design challenges. There is significant Variability in the manufacturing process for advanced technology nodes -> Analog design must compensate for all of these effects to ensure three basic qualities:-·) fidelity / Pxecision · Consistency · Performance

How to design Analog Circuits:-Analog IC design typically involves a top-down design and implementation process followed by a bottom - up verification process.

> Hose ose the basic steps -

.) Develop a high level specification for the design. What function will it portoom? What are the portormance, power and area (Cast) targets for the design?

Develop a top level design to achieve the required results using macro-functions such as filters,

Composators and amplifiers.

·) Create the device level circuit descriptions to support the top level design using component such as resistors

transistors and Capacitors.

· Verify that the design declivers on all its specification using simulation. The software used have will typically model the circuit using linear and non-linear clements that have been tuned for the targest fabrication process.

- It is during this step that manufacturing process and operational variability will be modeled to ensure the device design remain robust in the face of

these uncertainties.

) Implement a physical layout of the design by assembling the pre-defined layouts of all Components. Dusing this step, the donsity of the

layout is optimized to minimize cost. - Validation that these rules are followed occurs during this step, which is called physical verification.

> The equivalent circuit is then extracted from the layout. The extracted design is also compared to the original design to ensure the correct devices were used and Connected Correctly. The process is called logic

verses schematic checking.

) Any structures required for testing the circuit are added during this phase as well. Once complete, the design is ready for either manufacturing or integration into a largor digital design.

Integrating analog designs into a larger digital design is referred to as AMS, or analog/mixed signal design.

Analyse the interfacing of Analog and Digital System.

Ans: In which first of all instructional objectives are: O know the interfacing of analog signal to microcontrollers/microprocessors.

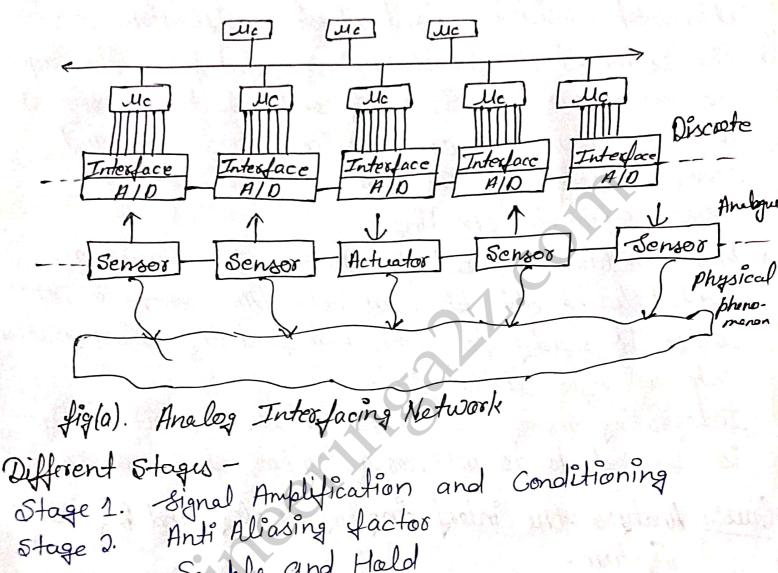
@ Generating Analog Signals

3 Designing AD and DA interface

1 Various methods of acquiring and generating analog

> In which below figure shows a typical sensor network you will find a number of sensors and actuates connected to common bus to phase information and

derive a collective decision. This is Complex embedded system. Digital camera falls under such a system.



Sample and Hold Stage 3.

Analog to Digital Convortes Stage 4.

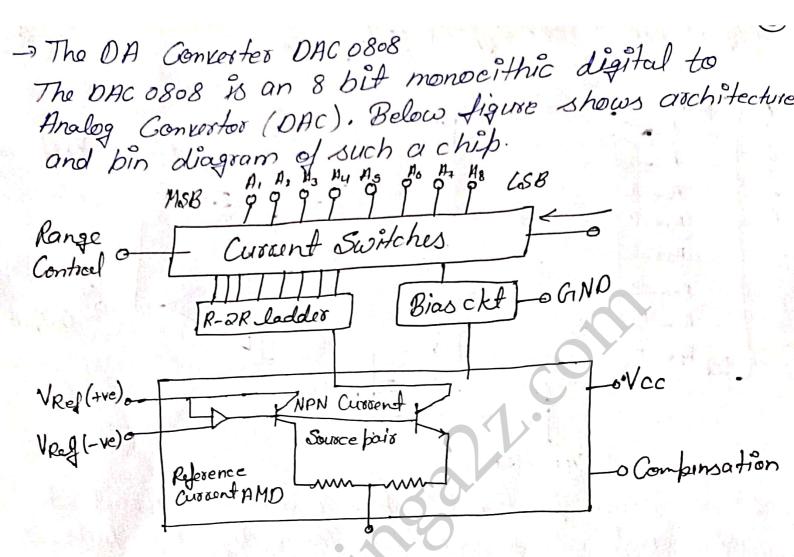
Digital Processing and Data Converter manipulation Stage 5. in a processor.

Processed Digital values are temporarily stored Stage b. îna latch before DA Conversion.

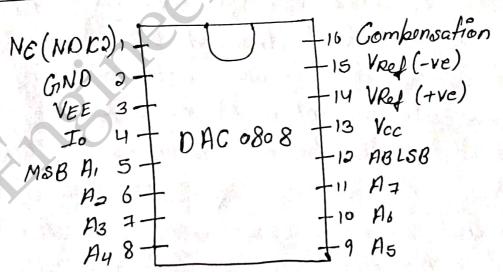
Digital to Analog Conversion Stage 7.

Removal of glitches and spikes Stage 8.

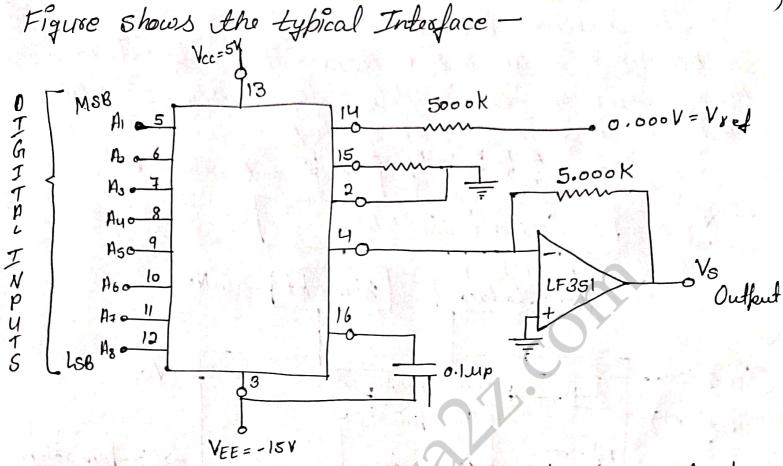
Final low pass filtering Stage 9.



## The DAC 0808 Signals



The O/A Converter has an output current, instead of an output veltage. An ob-amp converts the current to a valtage. The output current from pin 4 ranges between 0 to Imax 255/256 when all the Inputs are also 1. The O/P of O/A Convertor takes place some time to setter.



LF351 is an operational Amplifier used as current to proportional voltage convertor. The 8 digital Inputs at A8-A, is conversed into proportional current at bin 4 of DAC. The reference voltage (10V) are supplied at bin 14 and 15 C grounded through resistance.

- -> Important specifications ± 0.19 % Error settling time: 15 ons slew rate -> 8 m A/Ve Power supply voltage range ± 4.5 V to ± 18 V Power Consumption: 33 m V @ ±5 V
- The Internal A/D Gonverters of 80196 family of processor the external microprocessor compatible A/D Gonverter. A typical 8-bit DA Converter Both the ADCs use successive approximation technique. ADCs are complex and therefore generation difficult VLSI ckts unsuitable for coexistence on the same chip. Sigma Delta need very high sampling rate.

That is all about intexpacing of Analog and Digital System.

Complex programmable Logic Devices (CPLDs): ->

Complex programmable legal devices which are suitable in cases where the logic delign has large no. of imputs and outputs. Actually the simple programmable logic devices such as PALS, EEPLDs and GALs etc have Limited no. of imput and output that can support upto about 32 total no. of imput and outputs only.

when the no of injuts and cutputs is still higher than the capacity of existing PLDs, it is necessary to moreove the density. If the PLDs are made large most in terms of imputs, output and product term they becomes slower due to capacitive effect, leakage current, decrease in speed, po board area increases etc. A the same time, this solution does not make any cost effective use of chip area. Homce instead of moreasing the imputs, outputs and AND terms, It is better to have multiple PLDs structure having proof-

complex programmable logic devices (CPLDs) are corriginated from this idea. CPLD is a collection of individuals PLDs on a single chip with a programmable interconnection structure that allows the PLDs to get connected as the user wants

Generally, 2-input NAND Gate are used for any diottal IC chip. A typical PAL has 8 macrocells, if each macrocell represents about to equivalent gates, then the PAL

com accomplate a circuit that needs up to about 160 getes. for chewit repursny a very large no of gates, CPLDs having large no of gates, CPLDs having large no of macrocalls con implement circuit of about 1,000

epievalent gates.

as shown in fig.1.

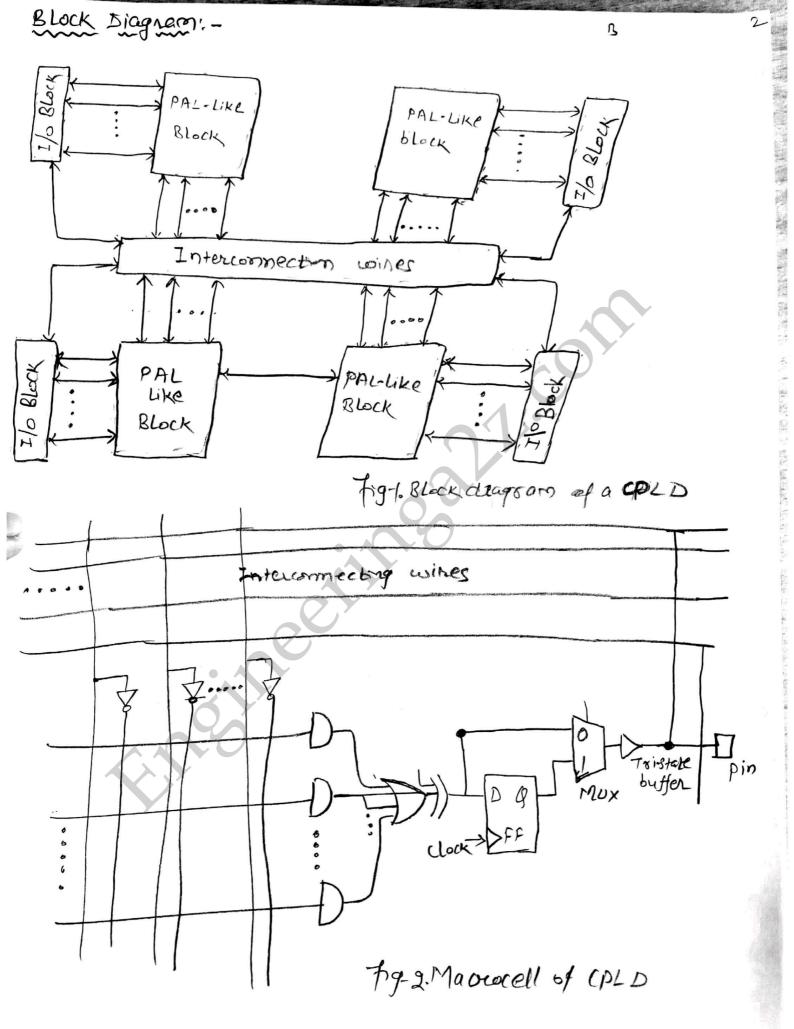


fig. 1 Shows the block abagram of a complex proopermmake device (CPLD). It consisted of number of PAL-Like
blocks, I/O blocks, and a set of intercommector wines.

\* the PAL Like blocks are connected to a set of interconnections wines and each block is also connected to
one input output (I/O) blocks to which a number of
chip's input and output pms are connected. attached.

- · A PAL- block combist of start 16 marzo cells. Each marso cells.
- · Each AND-OR configuration consist of 5-20 AND Grates and on or gate with 5-20 mputs.
- · An Ex-OR gate is used to obtain the out of OR Grate in inverted or non inverted form depending upon its other i/p beings nor o resp.
- · A D-FF stores the output of the Ex-or gate
- of the Ex-or gate depending upon its select input (1000)
- me to state buffer acts as a switch which enables the chip's pin to be used either as an autiput (toi-state enabled) or as an imput (toi-state-disabled). In case the chip's pin is used as an imput pin, an external source can drive a signer on to the pin which can be connected to the other macrocally using the interconnection wine, when it is used as an imput pin the macrocall becomes redundant and it is wested.

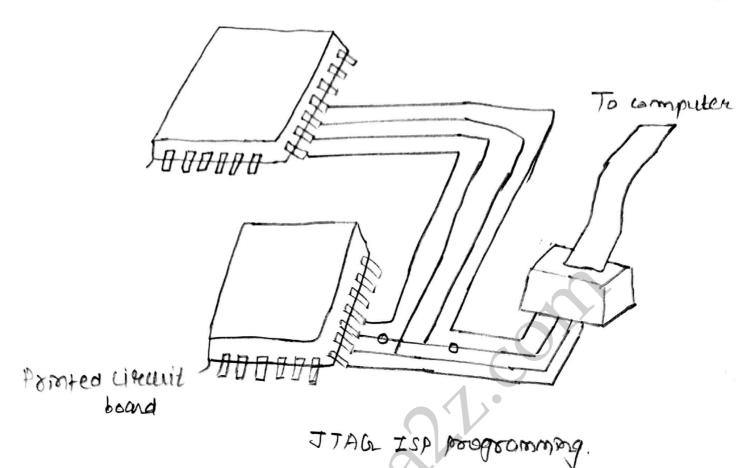
Programmable Legge devices SPLDs and CPLDS

the implemented using electrically exactable programmable head only memory (Efpron) technology. These are programmable townsed in the same usey as Efproms. The SPLD Chips have small no. of pins and can therefore be taken out of the cincuit board without any disturbance. In case of CPLDs, mestead of relying on a proportioning, a chip is attached to the cincuit board itself and this method of proportioning is known as in system programmap (ISP). There are many following reason to emopley the ISP:-

chip package and these pins can be easily bent.

· A socket 19 reprined to hold the chip in a programming

for programming SPLDs and CPLDs a large no of 8 wo; techen are repuired therefor it is difficult to operate commily due to large no of switches. So a computer Aided desting (CAD) system is employed . By using this CAD tool, a programming file or fure map 18 Jemerated that specifies the State of each switch. A computer system that own the can tool 18 connected by a cable to the programming unit. In case of ISP technique a small commecter is modulated on the PCB that houses the CPLD and computer system is Connected by a cable to this connected as shown in ity. bushaumuld surelines from Etomuld the besteamout file generated by the CAD system from the computer into the CPLD through this cable. The ancuitry on the CPLD that allow in system programming 18 usually called as JIAG pent. JTAG stonds for joint test action group. It uses four wines to transfer information b/w the computer and the device being programmed.



Quesil. Explain Embedded System.

Ans: Embedded system means semething that is attached to another thing. An Embedded system can be thought of as a computer hardware system having software embedded in it. An embedded system can be an independent system as it can be past of a large system. It is a micro controller as microprocessor based system which is designed to perform a specific task.

Characteristics of Embedded system

O single functioned - An embedded system usually performs a specialised operation and does the same repeatedly.

ed on design metrics, but those on an embedded

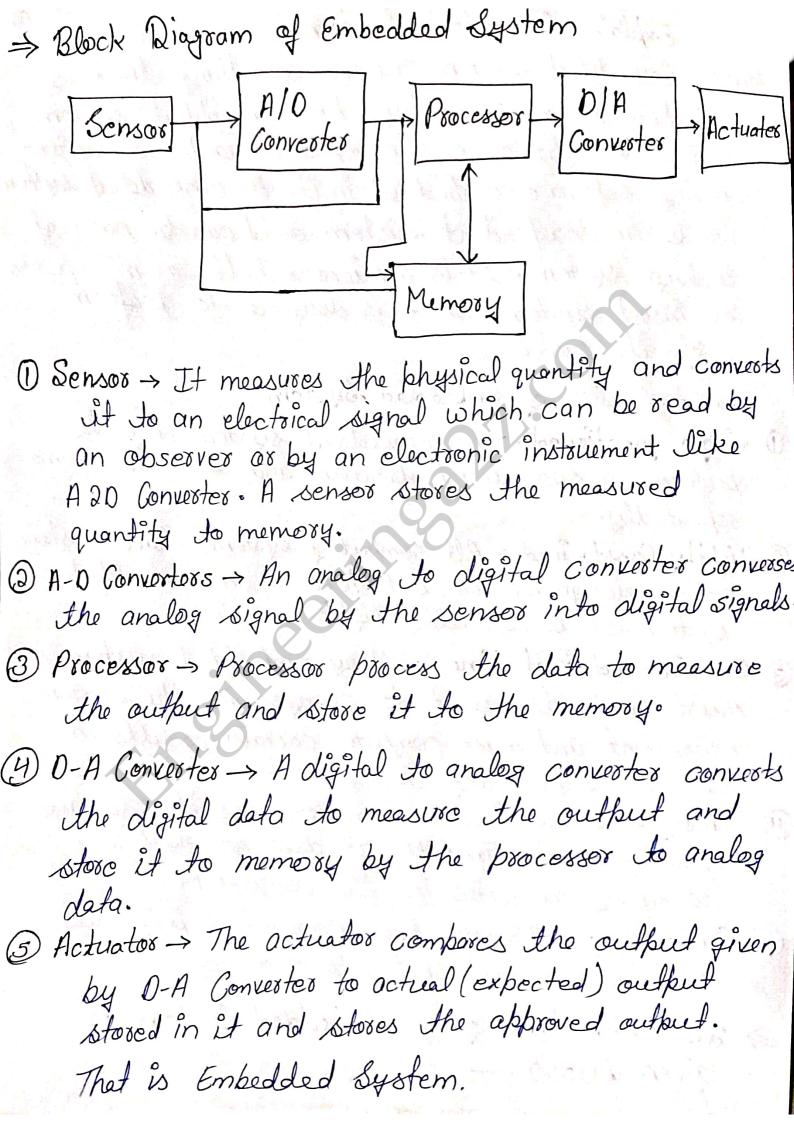
system can be specially tight.

3 Reactive and Real time -> Many embedded system must continually react to changes in the system's envisonment and must compute certain results in real time without any delay.

(4) Memory is It will have a memory, as its software usually embeds in ROM. It does not need any secondary memories in the competer.

(5) Connected -> It must have connected posipherals to connect Input and Output devices.

Basic Structure of an Embedded System is given below —



From the conditions (iii) and (iv), we observe that the OR gate is avoided and therefore, it becomes a high speed path. In this way, p-term passes through the EX-OR gate rather than sum term which saves typically 0.3 ns delay time of the OR gate. This path is especially useful for microprocessor address decoding for fast operation. This approach can also be used to build faster shift registers, counters, and some simple state machines.

## Design Security

In CoolRunner-II CPLD designs can be secured during programming using four independent levels of security provided on-chip. This eliminates any electrical or visual detection of configuration patterns, which prevents either any accidental overwriting or pattern theft via readback. The security bits programmed can be reset only by erasing the entire chip.

## In-system programming

All CoolRunner-II CPLD parts are 1.8 V in-system programmable. They derive their programming voltage and currents from the 1.8 V  $V_{\rm CC}$  on the part.

# 12.6 FIELD-PROGRAMMABLE GATE ARRAY (FPGA)

The programmable logic devices (SPLDs and CPLDs) are based on similar basic architecture—the programmable array logic (PAL) or the programmable logic array (PLA). Over the years, programmable arrays have increased in size and complexity, and highly configurable output macrocells have been added to enhance their flexibility and expandability. To increase the effective size and to add more functionality in a single programmable device, alternative architectures have been developed which are known as field-programmable gate arrays (FPGAs). The logic densities of FPGAs are much higher than those of CPLDs. They range in size from a few thousands to hundreds of thousands equivalent gates. From modern standards digital circuits with hundreds of thousands of gates is not too large. FPGA devices support implementation of relatively large complex logic circuits.

The FPGAs do not contain AND, OR planes, instead they provide logic blocks for implementation of the required digital functions.

An FPGA is composed of a number of relatively independent configurable logic blocks (CLBs), configurable I/O blocks, and programmable interconnection paths (known as routing channels). All the resources of the device are uncommitted and that these must be selected, configured and interconnected by a user to form a logic circuit for his application. The basic architecture of an FPGA is shown in Fig. 12.45.

There are a number of manufacturers of FPGA devices. The various families of FPGAs manufactured by different manufacturers differ primarily in the number of logic modules (from few hundreds to hundreds of thousands), supply voltage range, power consumption, speed, architecture, process technology, number of pins, and type of packages, etc. Some of the major manufacturers of FPGAs manufacturing a wide range of products to suit various types of requirements are given in Table 12.8.

The basic FPGA architecture consists of an array of configurable logic blocks (CLBs). The logic blocks are surrounded by configurable input/output blocks. There are rows and columns of programmable interconnection paths. The I/O blocks can be individually configured as input, output, or bidirectional.

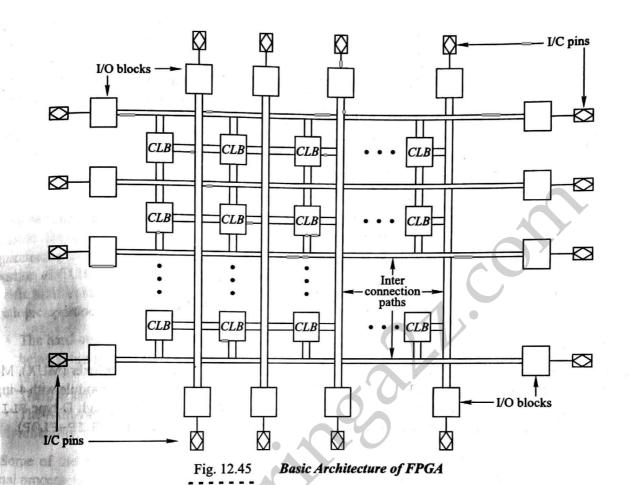


Table 12.8 FPGA Manufacturers

Manufacturer	FPGA products		www locator
Actel	Act 1, 2, 3, IGLOO	age 4	http://www.actel.com
Altera	Flex 6000, 8000, 10K, APEX 20K, Stratix II, III, IV		http://www.altera.com
Atmel	AT6000, AT40K		http://www.atmel.com
Lucent	Lattice SC, ECP2, XP2	My 21s	http://www.lucent.com
Quick Logic	PASIC 1, 2, 3, Eclipse	8	http://www.quicklogic.com
Vantis	VF1		http://www.vantis.com
Xilinx	XC4000, XC5200, Virtex, Spartan		http://www.xilinx.com

# Configurable Logic Blocks

There are a number of configurable logic blocks (CLBs) in an FPGA organized as an array of rows and columns. The logic blocks are connected to the I/O blocks through common row/column programmable interconnects. The common row/column interconnects are known as global interconnects. A logic block consists of a number of logic modules (LMs). The logic modules are the basic logic elements in an FPGA. The logic modules within a CLB are connected through local programmable interconnects. Figure 12.46 shows a CLB.

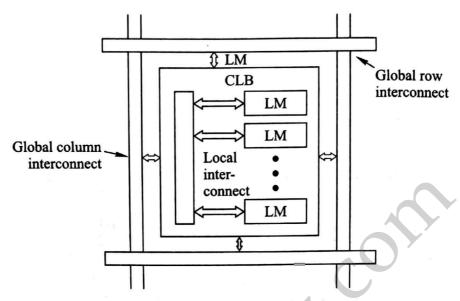


Fig. 12.46 Basic Configurable Logic Block

### Logic Module

A logic module consists of an LUT (look-up table), a D-type FLIP-FLOP and a mutliplexer (MUX). Most of the FPGAs are based on 4-input LUT. Figure 12.47 shows a block diagram of a logic module with 4-input LUT. Output of the LUT becomes the output of the logic module either directly or through D-type FLIP-FLOP. Thus, the output can be configured for combinational or registered (i.e., through FLIP-FLOP).

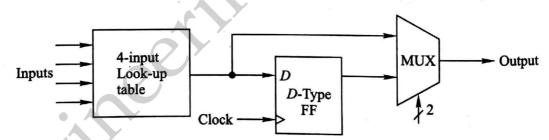


Fig. 12.47 Block Diagram of a Logic Module

# Look-Up Table (LUT)

An LUT (look-up table) consists of a programmable memory and it can be used to generate logic function in SOP form. For example, from Table 11.4, we can see that this table is similar to a 4-input and one output logic circuit's truth table. Therefore, a memory can generate canonical product terms. Figure 12.48 shows a block diagram of an LUT. It consists of a memory and a multiplexer (MUX). Let us assume the memory contents as given in the figure. Since, it is an 8-bit memory, therefore an 8:1 multiplexer is required. If the 3-bit logical input is  $A_2 A_1 A_0$ , then

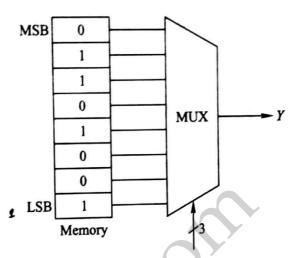
$$Y = \overline{A}_{2} \, \overline{A}_{1} A_{0} + \overline{A}_{2} A_{1} \, \overline{A}_{0} + A_{2} \, \overline{A}_{1} \, \overline{A}_{0} + A_{2} A_{1} \, A_{0}$$

The look-up table in most of the commercially available FPGAs is 4-input circuit. Larger LUTs would allow for more complex logic to be performed per logic block, thus reducing the wiring delay between blocks as fewer blocks would be needed. This will require larger multiplexer and an increased chance of waste if all of the functionality of the larger LUTs were not to be used. On the other hand, smaller look-up tables

may require a design to consume a large number of logic blocks, thus increasing wiring delay between blocks while reducing per logic block delay. Therefore, 4-input LUT structure makes the best trade-off between area and delay for a wide range of circuits. However, some of the latest FPGAs have been designed with 6-input LUT structure. The Xilinx Virtex-5 family of FPGAs have used 6-input LUT technology.

### FPGA Cores

A commercially available FPGA may have all the CLBs available for a user to program them according to his requirements. However, some FPGAs are available in which a portion of CLBs is used by the manufacturer to provide a



Block Diagram of an LUT Fig. 12.48

specific built-in function that can not be changed by a user. This is referred to as hard-core logic. The hardcore logic approach has the following advantages:

- The hard-core logic may normally be implemented using lesser number of CLBs than the same logic being programmed by a user. This saves the available chip resources, i.e., programmable area to the
- There is saving in the development time of user in developing a digital system.
- The built-in hard-core function can be thoroughly tested by the manufacturer, thereby increasing its

Some of the commonly used functions, such as microprocessors, standard I/O interfaces, and digital signal processors (DSPs) are available in hard-core FPGAs. Since the hard-core designs are developed by the manufacturers', therefore, these are the manufacturers' intellectual property (IP).

In case, the manufacturer's programmed function has some programmable features also, it is known as a soft-core function. Some intellectual properties may be combination of both hard-core and soft-core functions. The FPGAs containing either or both hard-core and soft-core embedded processors and other functions are known as the platform FPGA because they can be used to implement an entire system without the need for any external devices.

# FPGA Process Technology

There are different process technologies used by various FPGA manufacturers. These are:

- SRAM technology—It is based on static memory technology. The CMOS devices are fabricated by this SRAM technology are in-system programmable (ISP) and are reprogrammable.

  The antifuse technology and these are in-system programmable.
- technology and the antifuse technology developed by Actel Corporation of America is used for

   Antifuse technology—The antifuse technology developed by Actel Corporation of America is used for
- Antifuse technology which are one-time programmable (OTP). processing CMOS 11 to may be one-time programmable (OTP) or ultraviolet erasable type of CMOS

  • EPROM technology—It may be one-time programmable (OTP) or ultraviolet erasable type of CMOS
- device.

   EEPROM technology—It is electrically erasable which may be in-system programmable type or off-
- System programmable type CMOS technology. system programmable in system programmable type.

  • Flash technology—It is a bipolar one-time programmable type.
- Flash technology—It is a bipolar one-time programmable FPGA.
   Fuse technology—It is a bipolar one-time programmable FPGA.

# Configuration Memory

Most of the modern FPGAs use SRAM. The SRAM bits are used to hold the user defined configuration values.

#### Xilinx Virtex FPGAs 12.6.1

The field-programmable gate array was invented by Xilinx in 1984 and they are the leading manufacturers of FPGA devices. There are two major lines of Xilinx FPGAs, Spartan and Virtex. The Extended Spartan-3A and the Virtex-5 families are the latest available FPGAs from Xilinx.

# Configurable Logic Blocks

There are a number of CLBs organised as an array. Each CLB contains multiple basic logic units called logic cells (LCs). The logic cells are same as the logic modules (LMs) discussed earlier. The logic cells are LUT based. Each logic cell consists of an LUT, a FLIP-FLOP, and a multiplexer. In the Virtex-4 family, XC4VLX200 FPGA has CLB array of 192X116 containing 200,448 logic cells. The number of LUTs and the internal registers, i.e., FLIP-FLOPs is 178,176 each. In the Virtex series of FPGAs there is a concept of slice. A CLB of Virtex-4 family of FPGAs consists of 89,088 slices. There are two LUTs and two FFs in each slice. A CLB is made up of four slices.

The Virtex-5 family of FPGAs has a maximum of 240 × 108 array of CLBs, 51,840 slices, each slice contain four LUTs and four FFs. A CLB of Virtex-5 family FPGAs is made up of two slices. The function generators are configurable as 6-input LUTs or dual-output 5-input LUTs.

In addition to function generators and storage elements (FFs), each slice in both of the above FPGA families, contain arithmetic logic gates, large multiplexers, and fast carry look-ahead chain.

# Configuration

The devices of Virtex family are configured by loading the bitstream into internal configuration memory in various modes.

### **IP** Cores

In these devices, there are IP cores for commonly used complex functions including DSP, bus interfaces, processors, and processor peripherals.

# Process Technology

The Virtex-4 family of FPGAs are produced using 90-nm copper CMOS process technology, whereas the Virtex-5 family of FPGAs are produced using 65-nm copper CMOS process technology.

#### Altera Stratix FPGAs 12.6.2

Altera Corporation of America is producing wide range of FPGAs to meet different requirements. The Stratix series of FPGAs started in 2002 with the introduction of Stratix family. Subsequently, Stratix GX(2003), Stratix II (2004), Stratix II GX (2005), Stratix III (2006) and Stratix IV (2008) were introduced in the years mentioned in parentheses along the family. The basics of Stratix II family of FPGAs have been chosen for discussion here.

Stratix FPGAs contain a two dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs) and various other blocks, such as memory block structures and digital signal processing (DSP).

# Logic Array Block (LAB)

The configurable logic block (CLB) is called as logic array block in Altera FPGAs. Each LAB consists of eight adaptive logic modules (ALMs). An ALM is the basic building block of logic for efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. In addition to eight ALMs, each LAB contains carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. The LAB structure is shown in Fig. 12.49. The local interconnect transfers signals between ALMS in the same LAB. The local interconnect is driven by column and row interconnects, ALM outputs in the same LAB, and neighbouring LABs from the left and right through the direct link connection. The direct link connection feature helps in minimising the use of row and column interconnects which increases the performance and flexibility. Multiple LABs are linked together via the global row and column interconnects.

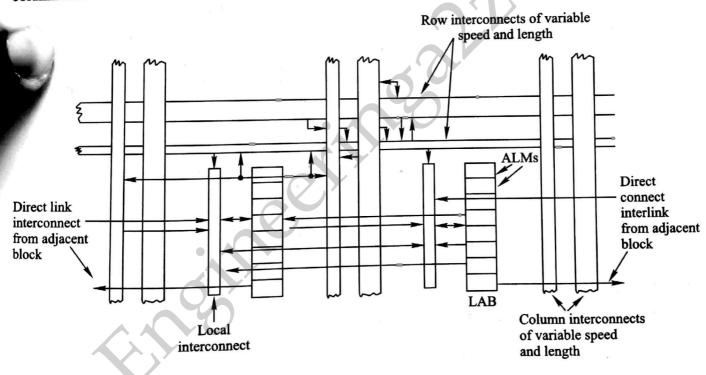


Fig. 12.49 Stratix II LAB Structure

# Adaptive Logic Modules (ALMs)

The basic building block of logic in these FPGAs is the adaptive logic module (ALM). Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). There are eight inputs in an ALM and one ALM can be used to implement various combinations of two functions including any function of upto six inputs and certain seven input functions.

In addition to the two ALUTs, each ALM contains two programmable registers (D-type FFs), two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Using these resources, the ALM can

implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, shared arithmetic chain, register chain, and direct connect interior global row and column, carry chain, shared arithmetic chain, register chain, and direct connect interlinks, and direct connect interlinks. The eight data inputs are: data a, data b, data Figure 12.50 shows block diagram of the ALM. The eight data inputs are: data a, data b, data c, data d Figure 12.50 shows block diagram of the first four data inputs, data a, data b, data c, and data d can be shared data f0, data e1, and data f1. The first four data inputs, data a, data b, data c, and data d can be shared data e 0, data t 0, data e 1, and data f 1. The most shared by the two LUTs, whereas data e 0 and data f 0 are dedicated to adder 0 and reg 0, and data e 1 and data f 1

Each ALM has two sets of outputs (combinational and registered) that drives the global and local routing resources. The combinational output can be either LUTs output or adder output. For combinational output the register is by passed. The registered output is obtained via the register. The two sets of outputs are

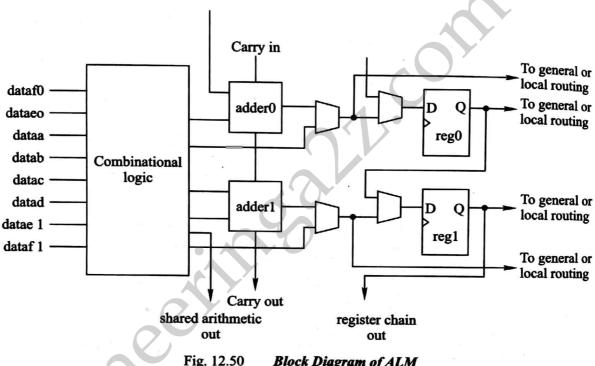


Fig. 12.50 **Block Diagram of ALM** 

### Operating Modes of ALM

The ALM of Stratix II can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Normal Mode In the normal mode combinational logic functions are generated. Two combinational functions in various combinations of 8 inputs can be implemented or a single function of upto six inputs can be implemented in this mode. Figure 12.51 shows the various combinations of logic functions generated using the two LUTs. In Figs. 12.51(a) and (b), the inputs are independent for the two LUTs, whereas in Figs. 12.51 (c), (d), and (f) 1, 2, and 4 inputs respectively are common between the two functions.

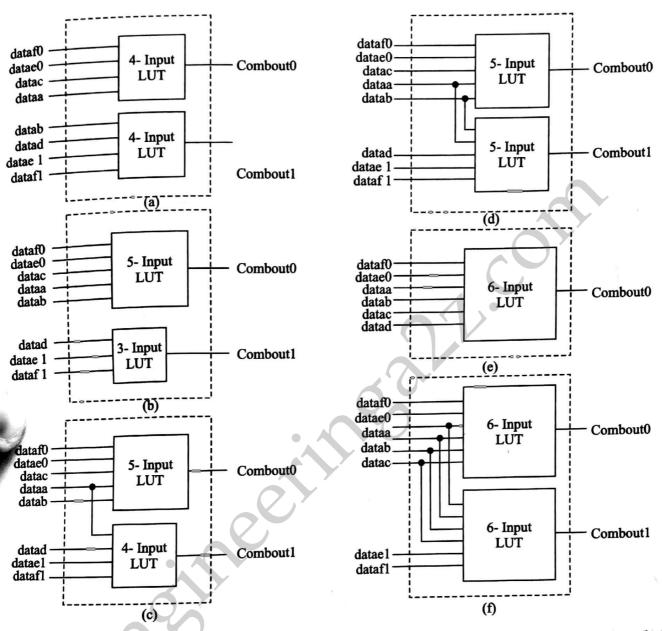


Fig. 12.51 Various Combinations of Logic Functions Generated using an ALM (a) Two 4-Input Functions (b) 5 and 3 Input Functions (c) 5 and 4 Input Functions (d) Two 5-Input Functions (e) 6-Input Functions (f) 6 and 2 Input Functions

Extended LUT Mode Some specific seven-input functions can be implemented by making two five input functions, sharing four inputs, and applying these two five-input functions to a 2:1 multiplexer. Figure 12.52 shows its implementation.

Arithmetic Mode The arithmetic mode is used for implementing adders, counters, accumulators, comparators, and parity functions. In arithmetic mode, an ALM uses two sets of two four-input LUTs alongwith two dedicated full adders.

Shared Arithmetic Mode In shared arithmetic mode, an ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs.

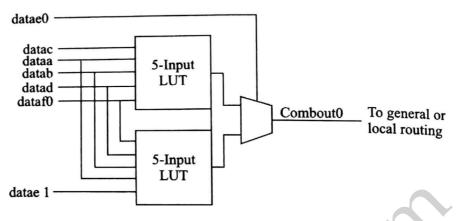


Fig. 12.52 Extended LUT Mode of an ALM

#### **SUMMARY**

The basic concepts of programmable logic devices and programmable gate arrays have been introduced. With the development of these devices, it has become possible to design complex digital systems. However, high-level design techniques and computer-aided tools are required to produce efficient PLD and FPGA implementations. Testing of PLD and FPGA implementations also require computer-assisted test tools. The design and test tools for these programmable devices are beyond the scope of this book.

The emergence of these devices has revolutionized the design of digital systems similar to the emergence of microprocessor. The programmable logic concept has emerged as a technology that has given the power to design one's own custom ICs which cannot be copied by others.

The design of embedded systems in small size has become possible by using FPGAs with intellectual properties, such as microprocessors, and DSP, etc. The embedded systems without using external devices and battery operated digital systems have proved very useful because of the availability of low-power FPGAs with intellectual properties.

#### **GLOSSARY**

Antifuse A programmable element invented by Actel Corporation named as PLICE (programmable low-impedance circuit element).

ASIC (Application specific integrated circuit) supplied by the user for a specific application.

An IC configured by the manufacturer as per the specifications

BGA (Ball grid array) An IC package used for ICs requiring large number of pins. The pins are of small round ball shapes.

CLB (Configurable logic block) A logic block in an FPGA consisting of logic modules and local programmable interconnect that is used to connect logic modules within the CLB to generate required logic functions.

Configuration memory A memory in an FPGA meant to store bit pattern for configuring the FPGA.

CPLD (Complex programmable logic device) A programmable logic device containing a large number of

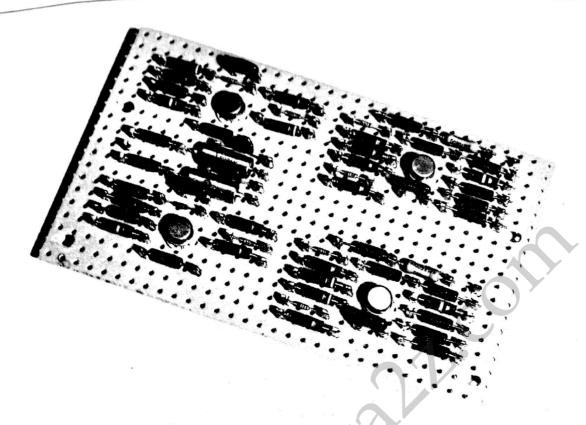


Figure 12.2. "Perfboard" can be handy for prototype circuits constructed with discrete components, although it is not particularly good for ICs. The terminals are press-fit into the holes (or flared with a special tool) and wired underneath.

of Wire-Wrap board is available with the pins on the component side of the board (the usual procedure is to have the pins stick out the other side). Although this type of board is less dense (fewer ICs per square inch), it is easier to use with discrete components, since you can see them while wrapping, and it allows closer spacing between adjacent circuit boards, since both components and Wire-Wrap pins take space on the same side. This kind of board without sockets is actually quite convenient for construction of linear or digital circuits. Figure 12.4 shows an example. In Figure 12.5 we have compared a prototype circuit built on a Wire-Wrap panel with the final printed-circuit version used in production. Printed circuits are much easier to produce in quantity; they are superior electrically and less cluttered than Wire-Wrap panels. We will talk about PC cards next.

#### PRINTED CIRCUITS

#### 12.04 PC board fabrication

The best method of constructing any electronic circuit in quantity is to use a printed circuit, a stable insulating sheet of material with thin plated copper lines bonded to the sheet forming the circuit paths. Although early printed circuits were associated with poor reliability (Remember the advertisements stressing the superior quality that only handcrafted television sets without printed circuits could provide?), the process of manufacturing board material and producing finished boards has been perfected to the point that printed-circuit boards now have very few problems. In fact, PC boards offer the most reliable fabrication technique. They are routinely used in computers, spacecraft, and military electronics where high reliability is essential.

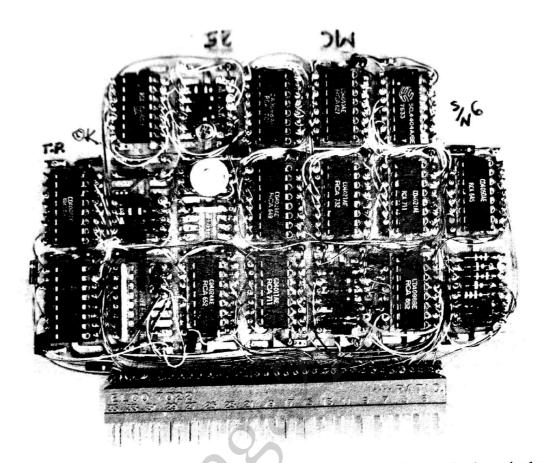


Figure 12.4. Wire-Wrap boards provide a neat and fast construction method particularly good for circuits made with digital ICs. This board uses a printed-circuit pattern to bring out the Wire-Wrap pins on the component side, an alternative to the usual underside pin configuration. Its peculiar shape is dictated by the interior of the oceanographic pressure cell into which it fits.

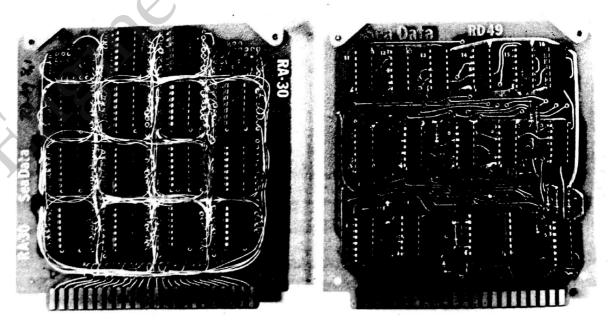


Figure 12.5. A Wire-Wrap prototype board and its printed-circuit successor. PC boards are less cluttered and far easier to fabricate in quantity. They eliminate wiring errors, too.

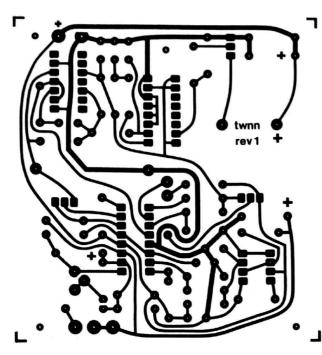


Figure 12.6. Foil pattern for a simple single-sided PC board. This "layer positive" was photographically reduced from a double-sized hand-taped Mylar pattern. The circuit board is 3.25×3.5 inches and has 4 ICs, 24 resistors, 11 capacitors, 5 diodes, 1 trimmer, and 1 piezo buzzer.

#### The "Mylar" or photoplot

Printed-circuit-board production begins with a set of actual-size transparencies on which an opaque pattern delineates the desired circuit traces and "pads" (Fig. 12.6). There are lots of rules and tricks in this business, but the basic idea is to figure out how to make all the interconnections the circuit demands by running lines around As we will describe shortly a board. (Section 12.08), these transparencies are usually produced directly on film by computer-driven photoplotters or laser plotters, working from a description of the circuit that you produce on a CAD (computer-aided design) system. However, for simple circuits, you may choose to do the layout manually, sticking opaque tape and patterns onto clear Mylar film. In the latter case you usually make the taped Mylar pattern twice actual size, from which you photographically produce an actual-size transparency.

No matter what the parentage of the final 1:1 transparency, the result is a set of conductor patterns on film. For the simplest boards you may be able to make all the needed connections (perhaps aided by a few wire "jumpers") with a singlesided board, which has all its traces on the underside (officially called the "solder" side; the top is called the "component" Most often, however, you need side). traces on both sides of the board. Such double-sided boards invariably use platedthrough holes (the holes in the board are lined with foil, connecting corresponding pads on both sides of the board). This really makes a difference when you are attempting to route traces, because you can always switch sides (using a "via" hole) when a trace runs into a dead end, whereas with a single-sided board you often get As an important hopelessly boxed in. side benefit, the use of plated-through holes ensures a superior solder joint to the component leads, because the solder wicks up through the hole.

For complex digital circuits you often see laminated multilayer PC boards, in which interior layers (called the "core") are used to carry ground and power-supply voltages, and sometimes signal lines as well. Four-layer and six-layer boards are pretty routine these days, with occasional use of more layers (up to 40!) in desperate situations.

#### Manufacturing

The board material (usually 1/16 inch of so-called FR-4 board, a fire-resistant epoxy-bonded fiberglass) comes clad on both sides with copper ("2 ounce" thickness is standard; the copper is 0.0027 inch thick). The first step is to drill the holes, using a template or automated drilling machine keyed to the full-size photopositive from the photoplotter or the Mylar

pattern. The holes are then "plated through" by a tricky multistep copper plating process, creating continuous conducting paths from one side of the board to the other.

The next step is to create a tough "resist" material, adhering to both sides of the board everywhere except where the foil for the circuit is to remain. This is done by (a) coating the board with a light-sensitive film (usually a thin adhesive "dry film"), then (b) exposing the board to light with the full-size photopositive accurately sandwiched on top, and (c) chemically "developing" the film (as in conventional photography) to make the exposed areas permanent. A step analogous to photographic "fixing" then removes the unexposed film, in precisely the pattern that will ultimately become the circuit traces. Then the board, with the pattern of resist now masking the areas where the copper foil is ultimately to be removed, is immersed into a solder-plating bath. result is to plate solder (a tin/lead alloy) everywhere that the foil pattern is to remain, including the insides of the holes.

Next the resist is removed chemically, exposing the copper that is to be removed, and the board is treated with a copperetching compound. That leaves the desired pattern of solder-plated copper, complete with plated-through holes. this point it is important to carry out a step known as "reflow soldering," which consists of heating the board to make the thin solder plating flow. This prevents the formation of tiny slivers of metal (from the undercutting action of the etching bath) that could otherwise cause conductive bridges. Reflow soldering also improves the solderability of the finished board; a reflow-soldered board is a delight to "stuff" with components.

The next step in board manufacture is to electroplate the edge-connector fingers with gold. The final process in board manufacture consists of applying a tough

"soldermask" coating over the entire board, covering all of the foil except for the pad areas. This greatly reduces the tendency to form "solder bridges" between closely spaced traces during subsequent soldering operations. It also makes the board moisture- and scratch-resistant. Soldermask materials can be applied by silkscreen methods ("wet mask") or by the same photographic "resist" methods used to create the foil circuit pattern ("dry mask"). You can recognize the soldermask by its dark green color and by the observed fact that it is practically impossible to remove. In industrial board manufacture. the board might then be stuffed by automatic machines, with all joints soldered in a few seconds in a "wave-soldering" machine. The alternative is to stuff and solder by hand.

There is a simpler process of board manufacture that is sometimes used, especially in small production situations or for singlesided boards, where plated-through holes aren't needed. In this method you begin by coating the board with photo-resist, then expose it through a full-size negative (rather than positive) of the desired pattern, i.e., a photographic film that is transparent wherever you want foil to remain. The resist is developed, and then the unexposed resist is dissolved away. This board then has a layer of tough resist covering the copper that is to remain, so you simply expose it directly to the etching compound (omitting the solder-plating step, above). After the superfluous copper has been etched away, the remaining resist is washed off with solvent, leaving the desired pattern in copper. At this point it is best to treat the board with an "electroless" tin-plating bath in order to cover the copper with a metal less susceptible to corrosion. As before, the edge-connector fingers will then be gold-plated. The final step in this process consists of drilling the holes by hand, using the actual conductive pattern as a guide (each "donut" pad has a small

opening in the center to aid in drilling the finished board).

#### ☐ 12.05 PC board design

There are several important decisions you have to make during PC board design, during component "stuffing," and finally when the board is used in an instrument. In this section we will try to touch on the most important of these.

#### □ PC board layout `

To make a printed-circuit board, you must ultimately convert your schematic diagram into a corresponding pattern of desired copper-foil traces that will compose the There are basically two finished board. (a) Working from the manually drawn schematics, you can use pencil and paper (and lots of erasers!) to figure out a set of interconnection paths ("routes") that does the job, then manually apply opaque tape and preformed connection patterns accurately onto clear polyester film to make the finished "Mylar" masters, or (b) you can convert your hand-drawn schematic to a connection "netlist," then use a CAD (computer-aided design) program to figure the trace routing, producing a set of precision machine-drawn "photoplots" directly; better still, you can replace the manual schematic drafting with CAD-based "schematic capture," in which you draw the diagrams directly on a graphics workstation, using a graphic tablet or mouse.

CAD-based circuit drawing and layout (option b, above) has many advantages, including automatic netlist extraction, painless documentation, the ability to check for design and layout rule errors, the ability to make changes relatively easily, and the ability to produce complex multilayer boards with precise alignment of pads and traces. It is the method of choice for nearly all complex and high-density PC board production. However, we would like

to begin simply, by briefly describing manual methods of PC board layout (option a, above). Once you know how to do a PC board layout by hand, you will understand what you're trying to make with the complex computer-based CAD tools. Furthermore, for simple jobs the manual methods may be all you need, and they are cheaper (and sometimes quicker) than CAD-based methods. They are particularly appropriate for the uncrowded boards you might use in simple unsophisticated instruments, of the sort you might build in small quantities for research laboratory use. They are also well adapted to boards containing parts with unusual shapes and lead spacings. Later, in Section 12.08, we will describe the CAD methods that are mandatory for high-density digital multilayer boards intended for large production.

There are several stages along the way from a schematic diagram to a final printed circuit. Beginning with the diagram, you trial pencil out generally work sketches of component layouts and interconnections, eventually working these together into a final pencil layout drawing. From this you make the "Mylar," consisting of accurately aligned "pads" (terminal areas for component connections) and taped interconnections. Precut patterns are used for IC and transistor pads and for ribbon and edge connectors, since these have standard spacings and dimensions. The pencil sketch and Mylar are usually made double size to allow greater accuracy (and to keep your eyes from popping out!). When the Mylar (two Mylars for double-sided boards) is completed, it is photographically reduced to an actualsize negative, from which a trial board is made as described previously. You generally "stuff" the prototype board with components, turn on the power, and then hunt down the errors; this lets you correct the Mylar artwork to produce final boards. The following subsections provide some further details and hints.

## ☐ Initial sketch

We recommend doing the initial layout with pencil on grid paper (5 lines/inch), with two colors to indicate foil patterns on the top and bottom (assuming it is a double-sided board). We usually use black pencil for runs on the bottom and green or red for the top (component) side. Since you're likely to do plenty of erasing, it is best to use vellum graph paper. The 0.2 inch gridding corresponds to 0.1 inch final size, the universal measure for IC pin spacings, transistor pinouts, edge connectors, etc. Your drawing should be the view from the component side; i.e., the sketch of the component-side (top-side) foil pattern looks like the final pattern, and the sketch of the bottom foil pattern is what you would see looking down through the finished board with x-ray eyes. While working on the layout, indicate component outlines with a pencil of a third color. All this work should be freehand. Don't waste time with an outline template; just use the grid lines as a guide to draw IC and component pinouts.

It is generally best to work up some trial layouts on a piece of scratch paper, particularly for sections of the circuit that may require special layout to minimize long lines or capacitive coupling. It may take some experimentation to arrive at good component arrangements. A trial layout might consist of a block of the circuit with two or three op-amps, or perhaps the input or output section of the circuit. These blocks should then be worked together onto the large gridded vellum, with adjustments being made as you go. Don't hesitate to do lots of erasing!

### ☐ Layout dimensions and hints

Try to have all ICs pointing in the same direction, preferably in straight rows. Likewise, resistors should be in even rows, not staggered. We use 0.030 or 0.040 black tape for signal runs, with wider tape for

power supplies (0.05 or 0.062 inch) and very wide ground runs (0.1 to 0.2 inch, or even wider; it's common to broaden the ground runs with lots of tape). Be sure to include plenty of bypass capacitors, one  $0.1\mu F$  for every two to four ICs. As you scratch your head, trying to juggle the tangled maze of interconnections, don't forget that components act as "jumpers" – they can hop over runs on the board.

Dimensions and spacings: On the actual-size PC board, we recommend holes spaced 0.4 inch for resistors ( $\frac{1}{4}$ W size). with spacing of 0.1 or 0.15 inch between resistors (with 0.15 inch spacing you can get a tape run between adjacent pads). We favor CK05 and CK06 types of ceramic capacitors, with their controlled 0.2 inch lead spacing, or the "DIP" 0.3 inch types (AVX type MD01, or Kemet C630C104M5U); they can also be spaced 0.1 inch from other capacitors or resistors. Leave some room around ICs for logic clips: a minimum of 0.2 inch to the next IC pads and a minimum of 0.15 inch to the nearest resistor or capacitor pads. Leave 0.030 inch spacing between tape runs, and don't run anything closer than 0.25 inch from the edge of the board, to allow room for card lifters, guides, standoffs, etc. Avoid running lines between the 0.1 inch spaced pads of an IC, unless necessary. You can fit up to six tape runs lengthwise between the pads of a standard DIP IC pattern (they're spaced 0.3 inch).

Recent PC design practice generally favors much higher line densities (both thinner lines and closer spacing) than the values recommended above; the latter would be called "15-15" design rules, signifying 0.015 inch minimum line width with 0.015 inch minimum conductor clearance. In the PC board industry, 15-15 rules are considered quite relaxed, with 12-12 pretty standard; 12-12 rules let you run one trace between adjacent IC pads on 0.1 inch centers (check for yourself that this is permitted, providing the pads aren't larger

than 0.064 inch in diameter). High-density boards often use 10-10 or 8-8 rules, with which you can squeeze two traces between adjacent IC pads (the maximum pad diameters are then 0.050 and 0.060 inch, respectively). Occasionally you see daring boards with 0.006 inch or thinner traces; the designers of such boards are trading the increased circuit density (three traces between adjacent pads, 20 down the center channel!) against smaller plated-through holes and other compromises that result in poorer production yield and board robustness.

#### ☐ Connections to the board

For the majority of boards it is probably best to bring out all connections through "edge-connector" contacts, which mate directly with sockets available in a variety of contact configurations. The most commonly used spacings are 0.156 inch, 0.125 inch, and 0.100 inch between fingers. Generally you'll put an edge-connector pattern at one end of the card, bringing power-supply voltages and signals through that connector. The card is mechanically supported, and it plugs in at that end (more on that shortly).

Often you see an edge-connector pattern at the other end of the card also, used instead of a flat ribbon connector to bring some other signals off the board or to other Another method for bringing boards. out signals is to use flat ribbon cable terminated in DIP plugs; such cables plug right into IC sockets on the board. You can buy these cables prefabricated in various lengths, or you can make them yourself with a kit consisting of flat cable, unassembled DIP plugs, and a crimping tool. Ribbon cables can also connect to the board via in-line or "mass-termination" connectors, which use one or two rows of pins on 0.1 inch centers.

For simple boards the best method of connection may be to use swage-solder

terminals or PC-type barrier strips with screw terminals. Avoid the use of large pads alone for connection of external wires to PC boards.

Figure 12.7 illustrates a variety of PC board connection techniques.

#### □ Odds and ends

With plated-through boards, use several holes to join ground foils on opposite sides of the board. Try to avoid using multiple passes through the board to reach your destination, since plated-through connections where no component is mounted are more likely to give trouble. The layout of a double-sided board generally winds up with most tape runs going horizontally on one side, vertically on the other.

General philosophy: Use smooth curves or 45° turns, rather than right-angle turns, for hand-taped layouts. Bring lines into pads as if heading for the center of the pad, rather than coming in at an oblique angle. Don't mount heavy components on boards (a couple of ounces ought to be the limit); assume that the instrument will be dropped 6 feet onto a hard surface Put polarity sometime during its life! markings on the component side for diodes and electrolytic capacitors, and label IC numbers and pin 1 location (if there's It is always nice to label test room). points, trimmer functions (e.g., "ZERO ADJ"), inputs and outputs, indicator light functions, etc., if you have room.

## ☐ Taping the Mylar

General advice: Use an illuminated "light table" with a piece of precision gridded Mylar taped to it. Don't confuse this with the inexpensive gridded plastic films that are neither accurate nor dimensionally stable; a piece of precision gridded film will set you back at least \$20. Put your clear Mylar over, and stick down the IC pads accurately on it. Use the pencil sketch for guidance while taping. Wash

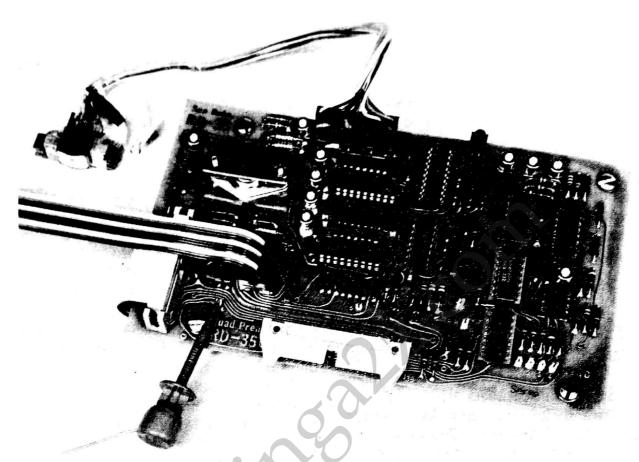


Figure 12.7. Several connection techniques are illustrated in this digital recorder printed-circuit card. The tape head connects via an in-line connector (which mates with a row of Wire-Wrap-type pins), and other signals are brought out with "mass-termination" ribbon connectors and a dual in-line ribbon connector. A test lead is shown clipped onto a "test point" terminal. This board also illustrates PC board heat sinking (upper left), a logic-state indicator (upper right), miniature single-turn trimmers, and single in-line (SIP) resistor networks.

your hands often to prevent deposition of oily film on the Mylar, and use alcohol to wipe any areas that might become oily. Use an Xacto knife with curved blade for tape and outline cutting, and learn not to cut through the Mylar. Press the tape down firmly after positioning; otherwise it will eventually curl up. Allow generous overlap where tape meets pad, etc. When laying out tape, don't hold it under tension; it will shrink and pull away from pads. Use precut bends and circles for the larger tape widths (0.062 inch or wider) when navigating tight turns. After the Mylar is completely taped, check it against the schematic by going over each connection on the diagram with a red pencil. When all seems OK, seal up

flaws on the Mylar with an indelible black felt-tip pen.

Precut PC graphics patterns are available from several manufacturers. Table 12.1 shows some recommended types. The Bishop Graphics catalog (5388 Sterling Center Drive, Westlake Village, CA 91359) includes extensive information on PC board layout and execution.

## 12.06 Stuffing PC boards

Your worries aren't over when you've got a finished board. You've got some decisions to make (e.g., whether or not to use IC sockets) and some important things to do (e.g., defluxing and lead trimming). Herewith, some thoughts on these subjects.

TABLE 12.1. SELECTED PC GRAPHIC PATTERNS

Pattern <sup>a</sup>	Bishop	Datak
Small pads (0.150" OD)	D203	JD-145
Medium pads (0.187" OD)	D104	JD-145
Large pads (0.250" OD)	D108	JD-140
Giant pads (0.300" OD)	D293	JD-343
	5200	00 040
0.150" thermal relief – pos	5272	JDS-532
0.150" thermal relief - neg	5278	-
	Accordance of the Control of the Con	
0.187" thermal relief – pos	5232	
0.187" thermal relief – neg	5238	_
16-pin DIP	6109	JD-64
16-pin DIP with in-betweens	6946	JD-179
20-pin DIP	6999	JD-575
20-pin DIP with in-betweens	-	JD-585
28-pin DIP	6904	JDS-398
28-pin DIP with in-betweens	· 1,	JDS-591
TO-5 transistor	6077	2.5
TO-18 transistor	6274	JD-88
TO-92 transistor	0274	JD-86 JD-91
10-32 (141131310)		00-31
0.100" connector pads	5004	JD-145
0.100" edge-connector strip	6714	JD-123
0.156" edge-connector strip	6722	JD-121
		0 # A
0.031" black tape	201-031-11	-
0.040" black tape	201-040-11	
0.050" black tape	201-050-11	
0.062" black tape	201-062-11	<b>7</b> - <b>7</b>
0.100" black tape	201-100-11	
0.200" black tape	201-200-11	_
	011004	_
0.062" universal corners	CU601 CU607	₩ -
0.100" universal corners	CU607	
0.200" universal corners	C0609	-
(a) for 2:1 artwork originals.		-

#### Sockets

There is great temptation to use IC sockets everywhere, for ease of troubleshooting. However, if you're not careful, the sockets may well cause more trouble than they prevent. In general, sockets are a good idea at the prototyping phase, where IC substitution may be necessary to convince you that the trouble you're having is a

design error, not a bad component. They should also be used for expensive ICs (e.g., a D/A converter, microprocessor, or the like), ICs that you're likely to want to change from time to time (e.g., a program ROM), and ICs that have a good chance of being damaged sooner or later (e.g., chips that buffer input or output signals from outside the instrument).

The problem is that a poorly designed socket may prove unreliable over extended time periods. A nonsoldered joint must have a gas-tight seal, such as that created by a mechanical metal-to-metal wiping action, with the seal then being left undisturbed. PC edge connectors, for example, used to be somewhat unreliable; with time, manufacturers learned some good tricks: bifurcated contacts (two independently sprung contacts for each finger), gold plating on the socket and on the edge fingers, and good mechanical design to ensure firm contact pressure during wiping and afterward. Joints that aren't gas-tight can be expected to fail after some time. perhaps a year or so. This sometimes happens inadvertently, e.g., by inserting a component in a PC board and then forgetting to solder it. Such connections have the maddening property of working fine at first, then becoming intermittent months or years later, owing to the formation of corrosion. A different problem can arise when heavy ICs (24 pins or more) are held in sockets. They can work their way out of the sockets after repeated vibration or shock.

We have found that the pin-and-jack type of IC socket (popularized by the Augat 5xx-AG series), although expensive compared with many other socket types, gives good reliability.

#### Soldering and defluxing

The usual procedure is to insert some components, turn the board over and bend the leads aside to hold the components